WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a) a plurality of interconnected circuit elements;

b) a number of scan chains which are interconnected with the plurality of interconnected circuit elements, said number of scan chains providing paths through which test data may be shifted into and/or out of the integrated circuit; and

c) current surge minimization circuitry which is interconnected with said plurality of interconnected circuit elements, whereby operation of said current surge minimization circuitry during operation of said number of scan chains minimizes current surges in said integrated circuit.

2. An integrated circuit as in claim 1, wherein:

a) said current surge minimization circuitry comprises a number of transistors which are coupled to ones of said plurality of interconnected circuit elements; and

b) said number of transistors receive a number of gating signals during operation of said number of scan chains, which number of gating signals disable current flow through the ones of said plurality of interconnected circuit elements.

3. An integrated circuit as in claim 2, wherein the current surge minimization circuitry comprises an electrical network connecting gates of the number of transistors to one or more external inputs of the integrated circuit, wherein the number of gating signals is applied to the number of transistors via application of one or more signals to said one or more external inputs.

4. An integrated circuit as in claim 3, wherein the electrical network

comprises a number of delay elements which cause a signal applied to one of said external inputs to be applied to the gates of various of said number of transistors at different times.

5. An integrated circuit as in claim 3, wherein the electrical network comprises a number of logic elements which cause at least one of said number of gating signals to change state in response to data shifted through at least one of said number of scan chains.

6. An integrated circuit as in claim 1, wherein:

a) the number of scan chains comprises at least first and second scan chains; and

b) the current surge minimization circuitry comprises distinct, external shift signal inputs corresponding to the first and second scan chains.

7. An integrated circuit as in claim 1, wherein:

a) the number of scan chains comprises at least first and second scan chains; and

b) the current surge minimization circuitry comprises a shift signal generator comprising a number of delay elements for delaying generation of a second shift signal with respect to generation of a first shift signal, said first shift signal being provided to a shift signal input of said first scan chain, and said second shift signal being provided to a shift signal input of said second scan chain.

8. An integrated circuit as in claim 7, wherein only one external input of said integrated circuit is coupled to a shift signal input of said shift signal generator.

9. An integrated circuit, comprising:

a) a plurality of interconnected circuit elements;

b) a number of scan chains which are interconnected with the plurality of interconnected circuit elements, said number of scan chains providing paths through which test data may be shifted into and/or out of the integrated circuit; and

c) means for minimizing current surges in said integrated circuit as said number of scan chains shift test data into and out of said plurality of interconnected circuit element.

10. An integrated circuit as in claim 9, wherein said means for minimizing current surges comprises means for gating out shift induced node state transitions in said integrated circuit as said number of scan chains shift test data.

11. An integrated circuit as in claim 9, wherein said means for minimizing current surges comprises means for phasing operation of at least two of said number of shift chains.

12. Logic synthesis software, comprising:

a) a number of computer readable media; and

b) computer readable program code stored on the number of computer readable media, the computer readable program code comprising:

i) program code for reading a circuit description file, the circuit description file comprising data which specifies current surge minimization constraints for a circuit which is described in the circuit description file;

ii) rules and design elements for minimizing current surges in a circuit; and

iii) program code for synthesizing current surge minimization circuitry using said design elements, in conformance with said current surge minimization constraints and said rules for minimizing current surges in a circuit.

13. Logic synthesis software as in claim 12, wherein the computer readable program code further comprises program code for synthesizing said circuit.

14. A method of designing an integrated circuit, comprising:

a) providing the integrated circuit with a number of scan chains which provide paths through which test data may be shifted into and/or out of the integrated circuit; and

b) providing the integrated circuit with current surge minimization circuitry.

15. A method as in claim 14, wherein said number of scan chains is at least two, and wherein providing the integrated circuit with current surge minimization circuitry comprises providing the integrated circuit with distinct external inputs for receiving shift signals corresponding to two different ones of said number of scan chains.

16. A method as in claim 14, wherein providing the integrated circuit with current surge minimization circuitry comprises providing the integrated circuit with a shift signal generator, said shift signal generator generating at least a first shift signal which i) is provided to a first of the number of scan chains, and ii) is out-of-phase with at least a second shift signal which is provided to a second of the number of scan chains.

17. A method as in claim 14, wherein providing the integrated circuit with current surge minimization circuitry comprises:

a) routing a number of gating signal lines to a number of circuit elements of the integrated circuit; and

b) routing each of said gating signal lines to an external input of the integrated circuit.

18. A method of testing an integrated circuit, comprising:

a) shifting test data through a number of scan chains of the integrated circuit; and

b) during at least a portion of said shifting, applying current surge minimization signals to the integrated circuit.

19. A method as in claim 18, wherein applying current surge minimization signals to the integrated circuit comprises applying gating signals to circuit elements of the integrated circuit.

20. A method as in claim 18, wherein applying current surge minimization signals comprises changing the state of at least one current surge minimization signal while said at least one current surge minimization signal is being applied.

21. A method of testing an integrated circuit, comprising:

a) providing test data to at least two scan chains of the integrated circuit; and

b) shifting test data through the at least two scan chains in parallel, but out-of-phase, while at least a portion of the test data is being provided to the at least two scan chains.

22. A method as in claim 21, wherein operating the at least two scan chains comprises:

a) providing at least a first shift signal to a first, but not a second, of the at least two scan chains; and

b) providing at least a second shift signal to the second, but not the first, of the at least two scan chains;

wherein the second shift signal is out-of-phase with the first shift signal.

23. A method as in claim 21, wherein operating the at least two scan chains comprises:

a) providing at least a first shift signal to a first of the at least two scan chains; and

b) providing at least a second shift signal to a second of the at least two scan chains;

wherein the first shift signal, the second shift signal, and any other shift signal provided to the first and second scan chains, are out-of-phase with respect to one another.